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EXAMINER	
JONES, ERIC W	

ART UNIT	PAPER NUMBER
2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,711	BLANCHARD, PIERRE	
	Examiner	Art Unit	
	ERIC W. JONES	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/12/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

2. Claims 26-30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected sensor, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 5/27/2008.

3. Applicant's election with traverse of claims 16-25 in the reply filed on 5/27/2008 is acknowledged. The traversal is on the ground(s) that 'product claims do not require backside thinning, where the process do.' This is not found persuasive because:

The process claims require 'etched layers on the active layer'; while the product claims require 'etched layers on the front face of the silicon layer.'

The active layer of the process claims does not have to be silicon; and the etched layers can be formed on either the front or back face of the active layer. Also, forming of the etched layers does not necessarily mean that they will be on the active layer; as the active layer can be anywhere in the layer, while the etched layers may be formed over areas not on the active area.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

4. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 27, 27, 28 and 29 have been renumbered 27, 28, 29 and 30.

5. Claims 23, 27, 29 and 30 are objected to because of the following informalities:

1. Claim 23 depends on a cancelled claim 1. For examination purposes, claim 23 depends on claim 16.

2. Claim 27 depends on a cancelled claim 11. For examination purposes, claim 27 depends on claim 26.

3. Claim 29 depends on a cancelled claim 11. For examination purposes, claim 29 depends on claim 26.

4. Claim 30 depends on a cancelled claim 14. For examination purposes, claim 30 depends on claim 29.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 19 recites the limitation "the metal layer" in line 1. There is insufficient antecedent basis for this limitation in the claim. There is no mention of any metal layer in claim 1. For examination purposes, 'the metal layer' is interpreted as the contact metal on the backside of the thinned wafer connected to the narrow vertical trenches.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 16-21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pourquier (US 6,960,483 B2) in view of Kirby et al (US 2005/0275049 A1).

Re claim 16, Pourquier (US 6,960,483 B2) discloses a process for the fabrication of electronic chips from a semiconductor wafer comprising, on its front face, a thin active layer of semiconductor material, the process comprising steps of:

formatting of etched layers (16 in FIG. 1) on the active layer (12 in FIG. 1); bonding the wafer (10 in FIG. 1) by its front face (FIG. 4) onto a support substrate

(20 in FIG. 3); thinning down of the semiconductor wafer via its backside (30 in FIG. 4); the depositing and etching of layers of material (18 in FIG. 5) on its backside thus thinned, wherein trenches (25 in FIG. 2) are etched into the wafer by its front face, before the bonding operation, these trenches extending into the wafer over a depth approximately equal to the residual semiconductor wafer thickness that will remain after the thinning operation (FIG. 4), the trenches being filled with a conducting material (14 in FIG. 2) isolated from the active layer and forming conducting vias between the front face and the backside of the thinned layer. (column 3, lines 12-67; column 4, lines 1-37; column 5, lines 1-9)

Pourquier (US 6,960,483 B2) fails to disclose narrow vertical trenches.

Kirby et al disclose narrow vertical trenches (through-wafer interconnects 226 in FIG. 2 and FIG. 6) for use in an image sensor (200 in FIG. 2 and FIG. 6). (pages 1-2, ¶ [0016]-¶ [0017], ¶ [0025]; page 5, ¶ [0054])

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the narrow vertical trenches (through-wafer interconnects) of Kirby et al with the trenches of Pourquier (US 6,960,483 B2) to couple device bond-pads to device ball-pads without mounting the imager to a separate, larger interposer substrate. (page 2, ¶ [0026])

Re claim 17, Pourquier (US 6,960,483 B2) discloses the trenches are formed before other deposition and etching steps of electrically functional layers on the front face of the semiconductor wafer. (column 3, lines 32-62)

Re claim 18, Pourquier (US 6,960,483 B2) fails to disclose the trench takes the form of an alignment marker visible from the backside after thinning in

order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face.

The recitation 'the trench takes the form of an alignment marker visible from the backside after thinning in order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face' is only a statement of the inherent properties of the 'process for the fabrication of electronic chips from a semiconductor wafer'. Once formed, the trenches can serve as alignment marks for subsequent backside device processing. The structure recited in Pourquier (US 6,960,483 B2) is substantially identical to that of the claims, claimed properties or functions, therefore, are presumed to be inherent. Or where the claimed and prior art products are produced by identical or substantially identical processes, a *prima facie* case of obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977). See MPEP § 2112.01.

Re claim 19, Pourquier (US 6,960,483 B2) discloses the metal layer (conductive boss 56 in FIG. 5) is deposited onto the backside of the wafer (30 in FIG. 5) after thinning, this layer being connected, by conducting vias (22 in FIG. 5) formed within at least one narrow trench, to at least one conducting layer (22 in FIG. 5) formed, prior to bonding the wafer onto the support substrate, on the front face of the wafer. (column 3, lines 12-67; column 4, lines 1-37; column 5, lines 10-18)

Re claim 20, Pourquier (US 6,960,483 B2) fails to disclose the metal layer is a photo- masking layer designed to prevent light impinging on photosensitive parts within an image sensor formed on the wafer.

The recitation 'is a photo- masking layer' is only a statement of the inherent properties of the 'process for the fabrication of electronic chips from a semiconductor wafer'. The conductive bosses are used for flip-chip bonding, and are generally made of solder, which blocks light (photo-mask). The structure recited in Pourquier (US 6,960,483 B2) is substantially identical to that of the claims, claimed properties or functions, therefore, are presumed to be inherent. Or where the claimed and prior art products are produced by identical or substantially identical processes, a *prima facie* case of obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977). See MPEP § 2112.01.

Re claim 21, Pourquier (US 6,960,483 B2) discloses layers of color filters are deposited onto the backside of the wafer after bonding and thinning. (column 5, lines 1-9)

Re claim 24, Pourquier (US 6,960,483 B2) discloses the role of trench (25 in FIG. 2) is to isolate laterally one portion of active layer from other portions of active layer (12 in FIGS. 1 and 2), and notably to isolate a region of active layer situated underneath an external connection pad (22 in FIG. 2) from the neighboring regions of active layer.

With respect to FIGS. 1 and 2, the trenches are formed between the active layers, thus isolating them from each other; and the trench isolates the external connection pad from the active layer.

11. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pourquier (US 6,960,483 B2) and Kirby et al as applied to claim 16 above, and further in view of Pourquier et al (US 7,217,590 B2).

Re claim 22, Pourquier (US 6,960,483 B2) and Kirby et al fail to disclose the semiconductor wafer and its support substrate are bonded onto another, transparent, substrate and the support substrate is eliminated.

Pourquier et al (US 7,217,590 B2) the semiconductor wafer (30 in FIG. 4) and its support substrate (20 in FIG. 4) are bonded onto another, transparent, substrate (80 in FIG. 7) and the support substrate is eliminated. (column 8, lines 33-62; column 9, lines 3-18)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the semiconductor wafer and its support substrate are bonded onto another, transparent, substrate and the support substrate is eliminated of Pourquier et al (US 7,217,590 B2) with the method of Pourquier (US 6,960,483 B2) and Kirby et al to produce connection pads flush with the conductive layers of the imager. (column 9, lines 15-18)

12. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pourquier (US 6,960,483 B2) and Kirby et al as applied to claim 16 above, and further in view of Bazan et al (US 6,515,317 B1).

Re claim 23, Pourquier (US 6,960,483 B2) discloses the trenches (25 in FIG. 2) have their internal walls coated with an insulator (26 in FIG. 2) and are filled with a metal (14 in FIG. 2). (column 3, lines 54-62)

Pourquier (US 6,960,483 B2) and Kirby et al fail to disclose a thin silicon oxide and highly doped polycrystalline silicon.

Bazan et al disclose trenches (FIG. 6) have their internal walls coated with thin (500 Å) silicon oxide (16 in FIG. 7 by thermal oxidation of silicon substrate) and are filled with polycrystalline silicon (7 in FIG. 7) that is highly doped ($1x10^{19}$ atoms/cm^3) so as to be conducting. (column 4, lines 26-40, 48-53, 65-67; column 5, lines 1-2; column 6, lines 31-34: claim 8)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the thin silicon oxide and polycrystalline silicon that is highly doped so as to be conducting of Bazan et al (US 7,217,590 B2) with the insulation and metal of Pourquier (US 6,960,483 B2) and Kirby et al to produce highly conductive interconnects.

13. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pourquier (US 6,960,483 B2) and Kirby et al as applied to claim 16 above, and further in view of Min (US 7,244,632 B2).

Re claim 25, Pourquier (US 6,960,483 B2) and Kirby et al fail to disclose the semiconductor wafer comprises a highly-doped silicon substrate coated with a more lightly doped epitaxial layer forming the active layer, of around 5 to 20 microns thickness, and in that the depth of the trenches is substantially equal to the thickness of the epitaxial layer.

Min discloses an image sensor comprising a highly-doped (p+) silicon substrate (10 in FIG. 4) coated with a more lightly doped (p-) epitaxial layer (11 in FIG. 4) forming the active layer, and forming trenches (41 in FIG. 4) in the active layer. (column 6, lines 40-62)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the highly-doped (p+) silicon substrate coated with a more lightly doped (p-) epitaxial layer forming the active layer, and forming trenches in the active layer of Min with the substrate, active layer, and the trenches of Pourquier (US 6,960,483 B2) and Kirby et al to produce an image sensor that easily senses red, green, and blue light via an optical wave within a depletion area. (column 3, lines 36-40)

Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the active layer, of around 5 to 20 microns thickness, and in that the depth of the trenches is substantially equal to the thickness of the epitaxial layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC W. JONES whose telephone number is (571)270-3416. The examiner can normally be reached on Monday-Friday 5:30AM-3:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571)272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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8/20/2008